IN THE CLAIMS

Please cancel claims 1-20 without prejudice.

Please add claims 21-40 as follows:

~~Patent Claims~~WHAT IS CLAIMED IS:

21. (New) A method for fabricating a memory device, including semiconductor structures with memory cells in which digital information is stored in a storage layer, the method comprising:

forming two source/drain regions which are spaced apart from one another by a channel region in a semiconductor substrate;

producing a gate dielectric on a substrate surface of the semiconductor substrate above the channel region;

arranging a first gate electrode on the gate dielectric;

forming the storage layer as an organic layer;

concluding processing of the semiconductor structures prior to application of the storage layer;

providing a conductive connection between the storage layer and the first gate electrode; and

arranging an insulator layer above the storage layer and arranging a second gate electrode on the insulator layer.

22. (New) The method of claim 21, further comprising arranging the storage layer between a first and a second electrode.

23. (New) The method as claimed in claim 22, further comprising forming the first electrode by a portion of the conductive connection.

24. (New) The method of claim 22, further comprising providing one metal from the group comprising aluminum, tungsten, and copper for the first and second electrodes.

25. (New) The method of claim 22, further comprising providing one precious metal from the group comprising Pt, Au, and Ag for the first and second electrodes.

26. (New) The method of claim 22, further comprising:

forming the first electrode in a first metal level and the second electrode in a second metal level; and

producing the conductive connection between the first gate electrode and the first electrode by filling a contact hole with conductive material.

27. (New) The method of claim 22, further comprising:

forming each of the first and second electrodes in a metal level which is in each case processed later in the process sequence; and

producing the conductive connection between the first electrode and the first gate electrode by contact holes arranged above one another and filled with conductive material.

28. (New) The method of claim 21, wherein the organic layer is provided having porphyrin molecules.

29. (New) The method of claim 21, wherein:

to produce source and drain lines, the source/drain regions of memory cells arranged in rows which are respectively adjacent within a row are electrically conductively connected to one another by doped regions provided in the semiconductor substrate; and

after a plurality of source/drain regions which have been electrically conductively connected to one another by doped regions in the semiconductor substrate, conductive

connections to interconnects, which are formed in a metal level and connect the source/drain regions of memory cells, are arranged.

30. (New) A memory cell comprising:

a storage layer that stores a digital information item;

two source/drain regions that are formed in a semiconductor substrate and that are spaced apart from one another by a channel region;

a gate dielectric arranged on a substrate surface of the semiconductor substrate above the channel region;

a first gate electrode arranged on the gate dielectric;

a conductive connection between the storage layer and the first gate electrode;

an insulator layer arranged above the storage layer, and a second gate electrode arranged on the insulator layer;

wherein the storage layer is formed as an organic layer; and

wherein the storage layer is arranged on the first gate electrode or at a distance from the first gate electrode.

31. (New) The memory cell of claim 30, wherein the storage layer is arranged between a first and a second electrode.

32. (New) The memory cell of claim 31, wherein the first electrode is formed by a portion of the conductive connection.

33. (New) The memory cell of claim 31, wherein the first and second electrodes consist of one of the group of metals comprising aluminum, tungsten, and copper.

34. (New) The memory cell of claims 31, wherein the first and second electrodes consist of one of the group of precious metals comprising Pt, Au, and Ag.

35. (New) The memory cell of claim 31, wherein:

the first electrode is formed in a first metal level and the second electrode is formed in a second metal level; and

the conductive connection between the first gate electrode and the first electrode is provided by a contact hole filled with conductive material.

36. (New) The memory cell of claim 31, wherein:

the first and second electrodes are each formed in a metal level which is in each case further away from the first gate electrode than the first or the second metal level; and

the conductive connection between the first electrode and the first gate electrode is formed by contact holes which have been introduced into insulation layers, are arranged above one another and have been filled with conductive material.

37. (New) The memory cell of claim 30, wherein the organic storage layer contains porphyrin molecules.

38. (New) A memory device comprising memory cells arranged in rows and semiconductor structures, and which store a digital information item, wherein the memory device includes memory cells comprising:

a storage layer that stores a digital information item;

two source/drain regions that are formed in a semiconductor substrate and that are spaced apart from one another by a channel region;

a gate dielectric arranged on a substrate surface of the semiconductor substrate above the channel region;

a first gate electrode arranged on the gate dielectric;

a conductive connection between the storage layer and the first gate electrode;

an insulator layer arranged above the storage layer, and a second gate electrode arranged on the insulator layer;

wherein the storage layer is formed as an organic layer; and

wherein the storage layer is arranged on the first gate electrode or at a distance from the first gate electrode.

39. (New) The memory device of claim 18, wherein:

to provide source and drain lines, source/drain regions of memory cells which are respectively adjacent in a row are electrically conductively connected to one another by doped regions provided in the semiconductor substrate; and

after a predetermined number of source/drain regions which have been electrically conductively connected to one another by doped regions in the semiconductor substrate, conductive connections to interconnects, which are formed in a metal level and connect the source/drain regions of memory cells, are arranged.

40. (New) A method for operating a memory device having:

a storage layer that stores a digital information item;

two source/drain regions that are formed in a semiconductor substrate and that are spaced apart from one another by a channel region;

a gate dielectric arranged on a substrate surface of the semiconductor substrate above the channel region;

a first gate electrode arranged on the gate dielectric;

a conductive connection between the storage layer and the first gate electrode;

an insulator layer arranged above the storage layer, and a second gate electrode arranged on the insulator layer;

wherein the storage layer is formed as an organic layer; and

wherein the storage layer is arranged on the first gate electrode or at a distance from the first gate electrode, the method comprising:

charging the respective storage layers of selected memory cells by means of an electron tunneling operation through the gate dielectric as a result of voltages being applied to the source/drain regions and the second gate electrode in order to program the memory device;

discharging the charged storage layers by means of an electron tunneling operation to the channel region or to the source/drain region as a result of an erase voltage, which differs from the voltage applied during programming, being applied to the second gate electrode in order to erase the programming; and

detecting the strength of a drain current as a function of a charge state of the storage layer in order to read the programmed memory device.